## REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated March 17, 2004. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 38-42 are under consideration. As outlined above, claim 38 is being amended to correct formal errors and to more particularly point out and distinctly claim the subject invention.

Additional Amendments

Claim 38 is being amended to correct formal errors and/or to better recite or describe the features of the present invention as claimed. All the amendments to the claim are supported by the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Prior Art Rejections

Claims 38-39, 41-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,284,644 to Aug et al. (hereinafter "Aug") in view of U.S. Pat. No. 6,627,554 B1 to Komada (hereinafter "Komada"), and claim 40 was rejected as being unpatentable over Aug in view of Komada, and further in view of U.S. Pat. No. 6,177,364 B1 to Huang (hereinafter "Huang"). This rejection has been carefully considered, but is most respectfully traversed.

The method of fabricating a semiconductor integrated circuit device according to the invention (e.g., Fig. 1; Explanatory Drawing 1; p. 15, first two paragraphs; Table 1, p. 23; "***dual damascene wirings*** *applied with Embodiment 1 and Fig. 3 to Fig. 7*" p. 23, lines 4-6), as now recited in claim 38, comprises: (a) forming a lower layer dielectric film 11 including a first silicon oxide film containing fluorine (e.g., SiOF) over a major surface of a wafer; (b) forming an upper layer dielectric film 15 including a second silicon oxide film substantially without fluorine (e.g., $SiO_2$) as compared with the first silicon oxide film 11 over the first silicon oxide film, the upper and lower layer dielectric films 11, 15 constituting an inter-layer

dielectric film having an *inter-wiring layer portion* embedded in the upper layer dielectric film 15 and *an inter-via layer portion* embedded in the lower layer dielectric film 11 respectively ("*Table 1 and Fig. 3 to Fig. 7 shows an example of dual damascene wirings using a silicon oxide film having a Young's modulus of about 70 GPa for the inter-wiring layer film and an SiOF film having a Young's modulus of about 50 GPa as the inter-via layer film*" p. 24, lines 5-8); (c) forming via holes 12 through said upper dielectric film 15 and said lower dielectric film 11 and then forming wiring grooves in the upper dielectric film 15, wherein at least one of said wiring grooves includes one of said via holes 12 in a groove pattern, said at least one of the wiring grooves and said one of said via holes 12 are connected therethrough, and said at least one of the wiring grooves has an area larger than an area of said one of said via holes 12 in plan view (Fig. 2); (d) forming a barrier metal along said wiring grooves and via holes 12 and then filling said at least one of the wiring grooves and said one of said via holes with copper so as to integrally form an embedded wiring 14 and a copper plug 13 electrically connecting the embedded wiring 14 to a lower wiring or electrode 10 ("*The connection member [via plug] for connecting the upper layer wirings and the lower layer wirings are formed integrally with the upper layer wirings.*" p. 28, last paragraph to p. 29). In particular, a Young's modulus of the lower dielectric film 11 (e.g., 50 GPa) is smaller than that of the upper dielectric film 15 (e.g., 70 GPa).

Accordingly, the copper wiring 14 in the wiring groove is surrounded by the upper dielectric layer 15 of a relatively large Young's modulus, and the via plug 13 in the via hole 12 is surrounded by the lower dielectric layer 11 of a relatively small Young's modulus. When the volume of the via plug 13 in the via hole 12 is expanded by thermal treatment, the elastic deformation of its surrounding lower dielectric layer 11 releasing the via hole expansion, while the upper dielectric layer 15 functions to suppress the volumic expansion of the wiring 14. As such, the via plug 13 is prevented from absorbing to the wiring 14 in the wiring groove due to the thermal treatment (p. 7, last paragraph to p. 8).

Applicants respectfully contend that Aug fails to teach or suggest forming such a via structure "having an *inter-wiring layer portion* embedded in the upper layer dielectric film 15 and *an inter-via layer portion* embedded in the lower layer dielectric film 11 of a relatively small Young's modulus" thereby preventing a via plug 13 from absorbing to the wiring 14 in the wiring groove due to the thermal treatment according to the invention.

In contrast, Aug's *inter-**wiring** layer portion* 12 is embedded in the FSG dielectric film 16 of a relatively *small* Young's modulus, rather than in the $SiO_2$ dielectric film 15 of a

relatively *large* Young's modulus according to the invention. Further more, Aug's ***inter-via*** *layer portion* 36 is embedded in both of the FSG dielectric film 16 and a TEOS dielectric film 22 of a relatively **large** Young's modulus (Fig. 8), rather than solely in the dielectric SiOF film 11 of a relatively **small** Young's modulus according to the invention. It is well established that a rejection based on cited references having principles that teach away from the invention is improper.

Aug only discloses a process of forming as via plug on a silicon substrate including : forming a first metal layer 12 of aluminum alloy (col. 3, line 26); forming a FSG layer 16 over first metal layer 12 (col. 3, line 36); exposing a surface of the FSG layer 16 to nitrogen plasma treatment 18 to convert the FSG to silicon nitride (col. 3, line 53); forming a TEOS silicon oxide film 22 on the FSG film 16 (col. 4, line 26); forming a via hole through the FSG layer 16 and the TEOS layer 22 to the first metal layer 12 (col. 4, line 39); and forming a via plug 36 of tungsten (col. 5, line 33).

Moreover, both Aug's *inter-**wiring** layer portion* 12 and Aug's *inter-**via** layer portion* 36 are surrounded by the same FSG dielectric film 16 of a relatively small Young's modulus close to their contacting interface. When the volume of the via plug in the via hole 36 is expanded by thermal treatment, even if the elastic deformation of the dielectric FSG layer 16 can partially releasing the via hole expansion of the lower section of the via plug, the upper section of the via plug supported by the TEOS dielectric film 22 suppress the volumic expansion of the upper section thus pushes the lower section of the via plug toward the wiring 12 anyway. As such, Aug's via structure only design to prevent outgassing from the FSG dielectric layer 16 (Abstract), but NOT to prevent its via plug from absorbing to the wiring 12 in the wiring groove due to the thermal treatment as the invention.

Kodama was relied upon by the Examiner to teach "forming a barrier metal along said wiring grooves and via holes." Kodama, however, fails to compensate for Aug's deficiencies. Kodama (Fig. 3A) merely discloses a process of forming a single damascene process formed on a tungsten via plugs, which includes the steps of: forming a first insulating film 4b of SiO film on a silicon substrate; forming a via hole 5 exposing a silicon substrate surface; forming a barrier metal 6 of TiN, a tungsten plug 7 in the via hole 5; forming a second insulating film 9 of SiO on the first insulating film 4b; forming a wiring trench 10 in the second insulating film 9; and forming a barrier metal 11 of TaN and copper 12 in the wiring trench 10.

In particular, Kodama's via plug 7 and the wiring are embedded in two SiO insulating films 4b, 9 of an identical Young's modulus, rather than in two insulating films of different

Young's moduli. Kodama forms the wiring and the via plug 7 separately with a metal 11 in-between (rather than contacting directly) such that Kodama need not to consider about any thermal stress to expend the tungsten via plug 7 into the wiring.

Huang was relied upon by the Examiner to teach "a SiC as stopper film" for dual damascene structure. Huang, however, also fails to compensate for Aug's deficiencies. Huang only discloses a method for forming an interlayer dielectric on a substrate including: forming a SiN or SiC film 110 on a substrate 105; forming a FSG film 120 on the SiN or SiC film 110; forming a SiC stopper firm 130 on the FSG film 120; forming a FSG film 140 on the SiC film 130; forming a SiN film 150 on the FSG film 140; and forming a wiring trench in a FSG film 140 and via hole in the FSG film 120.

Huang uses FSG films 120, 140 of an identical Young's modulus (rather than two insulating films of different Young's moduli) for a via plug and a wiring trench respectively such that the via structure can nit release the thermal stress to the via plug as the invention.

Applicants contend that neither Aug, nor its combinations with other cited references teaches or discloses each and every feature of the present invention as disclosed in independent claim 38. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance

of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

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